

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

- 1 1. (Currently Amended) An input buffer receiver comprising:
 - 2 a buffer input portion for receiving an input signal, said buffer input portion
 - 3 comprising a bias node;
 - 4 a large capacitor coupled between the bias node and a lower supply
 - 5 voltage ~~said large capacitor~~ for providing a coupling ratio between said
 - 6 large capacitor and a parasitic capacitor coupled between said bias
 - 7 node and a ground reference point ~~approaching~~ is approximately equal
 - 8 to a unity value such that a biasing voltage at said biasing node follows
 - 9 said lower supply voltage to minimize effects of a ground noise signal
 - 10 between the lower supply voltage and the ground reference point; and
 - 11 a buffer output portion in communication with the buffer input portion for
 - 12 producing an output signal.
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- 1 2. (Currently Amended) The input buffer receiver of claim 1, wherein the
 - 2 buffer input portion which receives the input signal further comprises:

3 a first transistor of a first conductivity type having a source node to which
4 the lower supply voltage is applied, a gate node to which a reference
5 voltage is applied, and a drain node at which the biasing voltage is
6 developed ;

7 a second transistor of a second conductivity type having a drain node
8 which is connected to the drain node of the first transistor, and a gate
9 node at which the biasing voltage is developed, and a source node to
10 which an upper supply voltage source is applied;

11 a third transistor of the second conductivity type having a drain node
12 which is connected to the drain of a fourth transistor, a gate node at
13 which the biasing voltage is developed, and a source node to which
14 the upper supply voltage source is applied;

15 a fourth transistor of the first conductivity type having a source node to
16 which the lower supply supply voltage is applied, a gate node to
17 which an the input signal is applied externally, and a drain node which
18 is an input to coupled to the drain of a fourth transistor and to an input
19 node of the buffer output portion.

- 1 3. (Previously Presented) The input buffer receiver of claim 2, wherein the
- 2 first and fourth transistors are NMOS transistors, and the second and third
- 3 transistors are PMOS transistors.
- 1 4. (Previously Presented) The input buffer receiver of claim 2, wherein the
- 2 large capacitor is connected between the sources of the first and fourth
- 3 transistors of the buffer input portion and the gate of the second transistor
- 4 of the buffer input portion.
- 1 5. (Previously Presented) The input buffer receiver of claim 2, wherein the
- 2 gate of the second transistor is connected to its drain.
- 1 6. (Previously Presented) The input buffer receiver of claim 2, wherein the
- 2 gate of the second transistor is connected to the drain of the first
- 3 transistor.
- 1 7. (Previously Presented) The input buffer receiver of claim 2, wherein the
- 2 gate of the second transistor is connected to the gate of the third
- 3 transistor.
- 1 8. (Currently Amended) The input buffer receiver of claim 2, wherein the
- 2 buffer output portion which produces the output signal comprises: a first
- 3 inverter connected to the drain of the third transistor and the drain of the
- 4 fourth transistor; transistor.

- 1 9. (Currently Amended) The input buffer receiver of claim 2, wherein the third
2 transistor and the fourth transistor activate and deactivate almost
3 simultaneously as determined by said input signal to minimize the effects
4 of ground noise on a delay jitter factor of said input buffer.

- 1 10. (Previously Presented) The input buffer receiver of claim 1, wherein the
2 large capacitor charge couples the bias node of the input buffer receiver to
3 the lower supply voltage of the input buffer receiver and wherein a
4 capacitance value of the large capacitor is selected by the formula:

$$\frac{CHC}{C_p + CHC} \approx 1$$

6 where:

7 . **CHC** is the capacitance value of the large capacitor,
8 and

9 Cp is the capacitance value of the parasitic capacitor.

- 1 11. (Currently Amended) The input buffer receiver of claim 1, wherein the
2 capacitance value of the large capacitor ~~relative to~~is chosen to be very
3 large with respect to a capacitance value of said parasitic capacitorand
4 results in a quicker response time for the output signal.

- 1 13. (Currently Amended) The integrated circuit of claim 12, wherein the buffer
2 input portion of the input buffer receiver further comprises:
3 a first transistor of a first conductivity type having a source node to which
4 the lower supply voltage is applied, a gate node to which a reference
5 voltage is applied, and a drain node at which the biasing voltage is
6 developed;
7 a second transistor of a second conductivity type having a drain node
8 which is connected to the drain node of the first transistor, and a gate
9 node at which the biasing voltage is developed, and a source node to
10 which an upper supply voltage source is applied;
11 a third transistor of the second conductivity type having a drain node
12 which is connected to the drain of a fourth transistor, a gate node at
13 which the biasing voltage is developed, and a source node to which
14 the upper supply voltage source is applied;
15 a fourth transistor of the first conductivity type having a source node to
16 which the lower supply voltage is applied, a gate node to which an
17 input signal is applied externally, and a drain node which is an input to
18 connected to the drain of a fourth transistor and to an input node of the
19 buffer output portion.

- 1 14. (Previously Presented) The integrated circuit of claim 13, wherein the first
- 2 and fourth transistors are NMOS transistors, and the second and third
- 3 transistors are PMOS transistors.
- 1 15. (Previously Presented) The integrated circuit of claim 13, wherein the
- 2 large capacitor is connected between the sources of the first and fourth
- 3 transistors of the buffer input portion and the gate of the second transistor
- 4 of the buffer input portion.
- 1 16. (Previously Presented) The integrated circuit of claim 13, wherein the gate
- 2 of the second transistor is connected to its drain.
- 1 17. (Previously Presented) The integrated circuit of claim 13, wherein the gate
- 2 of the second transistor is connected to the drain of the first transistor.
- 1 18. (Previously Presented) The integrated circuit of claim 13, wherein the gate
- 2 of the second transistor is connected to the gate of the third transistor.
- 1 19. (Currently Amended) The integrated circuit of claim 13, wherein the buffer
- 2 output portion which produces said output signal comprises: a first inverter
- 3 connected to the drain of the third transistor and the drain of the fourth
- 4 transistor; transistor.

1 20. (Currently Amended) The integrated circuit of claim 13, wherein the third
2 transistor and the fourth transistor activate and deactivate almost
3 simultaneously as determined by said input signal to minimize the effects
4 of ground noise on a delay jitter factor of said input buffer.

1 21. (Previously Presented) The integrated circuit of claim 12, wherein the
2 large capacitor charge couples the bias node of the input buffer receiver to
3 the lower supply voltage of the input buffer receiver and wherein a
4 capacitance value of the large capacitor is selected by the formula:

$$\frac{CHC}{Cp + CHC} \approx 1$$

6 where:

7 CHC is the capacitance value of the large capacitor,
8 and

9 Cp is the capacitance value of the parasitic capacitor.

1 22. (Currently Amended) The integrated circuit of claim 12, wherein the
2 capacitance value of the large capacitor relative to is chosen to be very
3 large with respect to a capacitance value of said parasitic capacitor and
4 results in a quicker response time for the output signal.

- 1 23. (Currently Amended) A method for minimizing effects of ground noise on
2 an input buffer receiver comprising the steps of:
3 forming a buffer input portion for receiving an input signal on a substrate;
4 forming a bias node within said buffer input portion;
5 connecting said a lower supply voltage to said buffer input portion;
6 forming a large capacitor coupled between the bias node and the lower
7 supply voltage ~~said large capacitor for~~ providing a coupling ratio
8 between said large capacitor and a parasitic capacitor coupled
9 between said bias node and a ground reference point ~~approaching-is~~
10 approximately equal to a unity value such that a biasing voltage at said
11 biasing node follows said lower supply voltage to minimize effects of
12 ~~[[a]] said~~ ground noise signal between the lower supply voltage and
13 the ground reference point; and
14 forming a buffer output portion on said substrate in communication with
15 the buffer input portion for producing an output signal.

- 1 24. (Currently Amended) The method of claim 23, wherein forming the buffer
2 input portion further comprises the steps of:
3 forming a first transistor of a first conductivity type on said substrate;

4 applying the lower supply voltage to a source node of the first transistor;

5 applying a reference voltage to a gate node of the first transistor;

6 connecting a drain node of the first transistor to develop [[as]] a biasing

7 voltage at said drain node;

8 forming a second transistor of a second conductivity type on said

9 substrate;

10 connecting a drain node of the second transistor to the drain node of the

11 first transistor;

12 connecting a gate node of the second transistor to the drain node of the

13 first transistor for developing the biasing voltage; and

14 connecting a source node of the second transistor to an upper supply

15 voltage;

16 forming a third transistor of the second conductivity type on said substrate;

17 ~~connecting a drain node of the third transistor to the drain of a fourth~~

18 ~~transistor;~~

19 connecting a gate node of the third transistor to the drain node of the first

20 transistor for developing the biasing voltage;

21 connecting a source node of the third transistor to the upper supply
22 voltage source;
23 forming a fourth transistor of the first conductivity type on said substrate;
24 connecting a source node of the fourth transistor to the lower supply
25 voltage;
26 connecting a gate node of the fourth transistor to receive an input signal
27 externally; and
28 connecting a drain node of the fourth transistor to an input to a drain node
29 of the third transistor and to an input node of the buffer output portion.

- 1 25. (Previously Presented) The method of claim 24, wherein the first and
2 fourth transistors are NMOS transistors, and the second and third
3 transistors are PMOS transistors.

1 26. (Previously Presented) The method of claim 24, wherein forming the large
2 capacitor comprises the step of:

3 connecting said large capacitor between the sources of the first and fourth
4 transistors of the buffer input portion and the gate of the second
5 transistor of the buffer input portion.

- 1 27. (Previously Presented) The method of claim 24, wherein forming the
- 2 buffer input portion further comprises the steps of:
- 3 connecting the gate of the second transistor to its drain.
- 1 28. (Previously Presented) The method of claim 24, wherein forming the
- 2 buffer input portion further comprises the steps of:
- 3 connecting the gate of the second transistor to the gate of the third
- 4 transistor.
- 1 29. (Currently Amended) The method of claim 24, wherein forming the buffer
- 2 output portion which ~~produces output~~ produces the output signal
- 3 comprises the step of:
- 4 forming a first inverter on said substrate; and
- 5 connecting an input of said first inverter to the drain of the third transistor
- 6 and the drain of the fourth ~~transistor~~ transistor.
- 1 30. (Currently Amended) The method of claim 24, wherein the third transistor
- 2 and the fourth transistor activate and deactivate almost simultaneously as
- 3 determined by said input signal to minimize the effects of ground noise on
- 4 a delay jitter factor of said input buffer.

- 1 31. (Previously Presented) The method of claim 23, wherein the large
2 capacitor charge couples the bias node of the input buffer receiver to the
3 lower supply voltage of the input buffer receiver and wherein a
4 capacitance value of the large capacitor is selected by the formula:

5
$$\frac{CHC}{Cp + CHC} \approx 1$$

6 where:

7 CHC is the capacitance value of the large capacitor,
8 and

9 Cp is the capacitance value of the parasitic capacitor.

- 1 32. (Currently Amended) The method of claim 23, wherein the capacitance
2 value of the large capacitor relative to is chosen to be very large with
3 respect to a capacitance value of said parasitic capacitor and results in a
4 quicker response time for the output signal.

- 1 33. (Currently Amended) An apparatus for minimizing effects of ground noise
2 on an input buffer receiver, said apparatus comprising:
3 means for forming a buffer input portion for receiving an input signal on a
4 substrate;

5 means for forming a bias node within said buffer input portion;

6 means for connecting said a lower supply voltage to said buffer input

7 portion;

8 means for forming a large capacitor between the bias node and the lower

9 supply voltage ~~said large capaciter for~~ providing a coupling ratio

10 between said large capacitor and a parasitic capacitor coupled

11 between said bias node and a ground reference point ~~approaching is~~

12 approximately equal to a unity value such that a biasing voltage at said

13 biasing node follows said lower supply voltage to minimize effects of

14 ~~[[a]] said~~ ground noise signal between the lower supply voltage and

15 the ground reference point; and

16 means for forming a buffer output portion on said substrate in

17 communication with the buffer input portion for producing an output

18 signal.

1 34. (Currently Amended) The apparatus of ~~claim 23~~ claim 33, wherein forming

2 the buffer input portion further comprises:

3 means for forming a first transistor of a first conductivity type on said

4 substrate;

5 means for applying the lower supply voltage to a source node of the first
6 transistor;

7 means for applying a reference voltage to a gate node of the first
8 transistor;

9 means for connecting a drain node of the first transistor to develop as
10 biasing voltage at said drain node;

11 means for forming a second transistor of a second conductivity type on
12 said substrate;

13 means for connecting a drain node of the second transistor to the drain
14 node of the first transistor;

15 means for connecting a gate node of the second transistor to the drain
16 node of the first transistor for developing the biasing voltage; and

17 means for connecting a source node of the second transistor to an upper
18 supply voltage;

19 means for forming a third transistor of the second conductivity type on said
20 substrate;

21 means for connecting a drain node of the third transistor to the drain of a
22 fourth transistor;

23 means for connecting a gate node of the third transistor to the drain node
24 of the first transistor for developing the biasing voltage;

25 means for connecting a source node of the third transistor to the upper
26 supply voltage source;

27 means for forming a fourth transistor of the first conductivity type on said
28 substrate;

29 means for connecting a source node of the fourth transistor to the lower
30 supply voltage;

31 means for connecting a gate node of the fourth transistor to receive [[an]]
32 said input signal externally; and

33 connecting a drain node of the fourth transistor to an input to a drain node
34 of the third transistor and to an input of the buffer output portion.

1 35. (Currently Amended) The apparatus of claim 24 claim 34, wherein the first
2 and fourth transistors are NMOS transistors, and the second and third
3 transistors are PMOS transistors.

1 36. (Currently Amended) The apparatus of ~~claim 24~~ claim 34, wherein means
2 for forming the large capacitor comprises:

3 means for connecting said large capacitor between the sources of the first
4 and fourth transistors of the buffer input portion and the gate of the
5 second transistor of the buffer input portion.

1 37. (Currently Amended) The apparatus of ~~claim 24~~ claim 34, wherein means
2 for forming the buffer input portion further comprises:

3 means for connecting the gate of the second transistor to its drain.

1 38. (Currently Amended) The apparatus of ~~claim 24~~ claim 34, wherein means
2 for forming the buffer input portion further comprises the steps of:

3 means for connecting the gate of the second transistor to the gate of the
4 third transistor.

1 39. (Currently Amended) The apparatus of ~~claim 24~~ claim 34, wherein means
2 for forming the buffer output portion which produces said output signal
3 comprises:

4 means for forming a first inverter on said substrate; and

5 means for connecting an input of said first inverter to the drain of the third
6 transistor and the drain of the fourth transistor; transistor.

1 40. (Currently Amended) The apparatus of ~~claim 24~~ claim 34, wherein the
2 third transistor and the fourth transistor activate and deactivate almost
3 simultaneously as determined by said input signal to minimize the effects
4 of ground noise on a delay jitter factor of said input buffer.

1 41. (Currently Amended) The apparatus of ~~claim 23~~ claim 33, wherein the
2 large capacitor charge couples the bias node of the input buffer receiver to
3 the lower supply voltage of the input buffer receiver and wherein a
4 capacitance value of the large capacitor is selected by the formula:

$$\frac{CHC}{Cp + CHC} \approx 1$$

6 where:

7 CHC is the capacitance value of the large capacitor
8 CHC, and

9 Cp is the capacitance value of the parasitic capacitor
10 Cp.

1 42. (Currently Amended) The apparatus of claim 23 claim 33, wherein the
2 capacitance value of the large capacitor relative to is chosen to be very
3 large with respect to a capacitance value of said parasitic capacitor and
4 results in a quicker response time for the output signal.